REMARKS

Claims 47 and 56 have been cancelled. Claims 39, 41-46, 48, 50-55, and 74 have been amended. Marked-up versions of amended claims 39, 41-46, 48, 50-55, and 74 are attached hereto. Claims 39, 41-46, 48, 50-55, 57, and 74 -83 are pending in the application. Applicant reserves the right to pursue the original claims and other claims in this application and in other applications.

Claims 39 and 41-46 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz et al., U.S. Patent No. 6,088,216 (hereinafter "Laibowitz"), in view of Azuma et al., U.S. Patent No. 5,516,363 (hereinafter "Azuma"). The rejection is respectfully traversed.

Claim 39, as amended, recites a capacitor having a "first level and a second level" connected by "at least two sidewall regions" and "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." According to the claim, the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." Applicant respectfully submits that Laibowitz and Azuma do not teach or suggest the claimed invention.

Laibowitz discloses a DRAM capacitor comprising a substrate 12, whereupon a mesa 51 and high dielectric film 56 are formed (Figure 7). However, Laibowitz fails to teach or suggest a capacitor in which the stoichiometry of the sidewalls is substantially uniform. Additionally, Laibowitz fails to disclose the importance of maintaining a uniform stoichiometry in the layer of thin film dielectric material on a sidewall. It should be noted that Laibowitz discloses a thin film material deposition technique and resulting structure upon which the claimed invention improves.

Azuma relates to a method of achieving uniform stoichiometry. Specifically, Azuma teaches doping "liquid precursor solutions for use in processes for forming thin-layer capacitors." (Abstract). The doped precursor solution is applied to a substrate,

"conducted by dropping the precursor solution onto substrate 18 and then spinning substrate 18 at about 1500 RPM (the preferred range is about 1500-2000 RPM) for about 30 seconds." (Col. 18, lines 4-8). Azuma fails to teach or suggest that its "spin coat" method could be used on three-dimensional (3D) material layers. Indeed, Azuma's FIG. 3 illustrates a flat substrate on which the precursor solution is being deposited.

Applicant respectfully submits that Laibowitz and Azuma are not properly combinable. The method taught by Azuma cannot be applied to Azuma's 3D structure resulting in a capacitor having "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level" and being "a continuous layer" because it involves a "spin-on" step.

The combination of Laibowitz and Azuma structure would result in a structure depicted in attached Figs. A and B. Referring to Fig. A, the "spin-on" method disclosed by Azuma would result in an accumulation of the pre-doped precursor solution on a near raised sidewall, while not covering at all the far raised sidewall. In the case of a deep trench (Fig. B), the pre-doped precursor solution would accumulate at the far lowered sidewall, while failing to cover the near lowered sidewall. Therefore, the combination of Laibowitz and Azuma would not result in a "continuous layer" over two sidewall regions and a second level, as recited in claim 39. In addition, because a continuous layer is cannot be formed using the "spin coat" method, "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level" cannot be achieved with the combination of Laibowitz and Azuma. The combination of Azuma and Laibowitz fails to teach or suggest every limitation of claim 39. For at least this reason, Applicant respectfully submits that claim 39 is allowable.

Claims 41-46 depend from claim 39. Claims 41-46 contain every limitation of claim 39, and are allowable along with claim 39. Accordingly, the rejection should be withdrawn and the claims allowed.

Claims 48 and 50-55 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Laibowitz, in view of Azuma, and further in view of Leung et al., U.S. Patent No. 5,563,762 (hereinafter "Leung"). The rejection is respectfully traversed.

Claim 48, as amended, recites a capacitor having a "first level and a second level" connected by "at least two sidewall regions" and "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." According to the claim, the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." A capping layer is also provided over at least a portion of said BST thin film material.

As noted above with respect to claim 39, Laibowitz and Azuma fail to teach or suggest a capacitor having a "continuous" "ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." Leung discloses preparation of a capacitor whereby "a capping layer is deposited overall to encapsulate the capacitor structure" (Col. 2, line 46-49). Leung does not, however, disclose a capacitor with uniform stoichiometry of the BST high dielectric constant thin film material. Accordingly, the combination of Laibowitz, Azuma and Leung fails to teach or suggest the subject matter defined in claim 48. For at least the foregoing reasons, claim 48 is allowable over the combination of Laibowitz, Azuma, and Leung.

Claims 50-55 depend from claim 48. Claim 50-55 contain every limitation of claim 48, and are allowable along with claim 48. Accordingly the rejection should be withdrawn and the claims allowed.

Claims 74-83 stand rejected under 35 U.S.C. § 103(a) as being unpatentable over Hosotani et al., U.S. Patent No. 6,051,859 (hereinafter "Hosotani") in view of Azuma. The rejection is respectfully traversed.

Claim 74, as amended, recites a capacitor having a first electrode having two sidewall regions and a second level and "an ion implantation doped BST high dielectric

constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level." The claim further recites that the ion implantation doped BST high dielectric constant thin film material is "a continuous layer at least on said two sidewall regions and said second level." A second electrode is provided on the BST high dielectric thin film material.

As noted above with respect to claims 39 and 48, Azuma fails to teach or suggest a capacitor comprising "a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions" and "an ion implantation doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over said at least two sidewall regions and over said second level" that is "a continuous layer at least on said two sidewall regions and said second level." Although Hosotani teaches a cup-shaped capacitor comprising a substrate, first electrode, dielectric film, and second electrode, it does not teach or suggest an ion implantation doped BST thin film material having a substantially uniform stoichiometry. As discussed above with respect to claim 39, Azuma is not properly combinable with a 3D structure (i.e., the Hosatani cup-shaped capacitor). Accordingly the combination of Azuma and Hosotani fails to teach or suggest the subject matter defined in claim 74. For at least the foregoing reasons, claim 74 is allowable over the combination of Azuma and Hosotani.

Claims 75-83 depend from claim 74. Claims 75-83 contain every limitation of claim 74, and are allowable along with claim 74. Accordingly the rejection should be withdrawn and the claims allowed.

In view of the above, each of the presently pending claims in this application is believed to be in immediate condition for allowance. Accordingly, the Examiner is respectfully requested to withdraw the outstanding rejection of the claims and to pass this application to issue.

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Respectfully submitted,

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Version With Markings to Show Changes Made

39. (Fifth Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation [a post deposition] doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over [at least on both] said at least two sidewall regions and over said second level;

wherein [the stoichiometry of] said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level [substantially uniform at least at both sidewall regions].

41. (Second Amended) The capacitor according to claim 39, wherein [said dopants] said ion implantation doped BST thin film material is doped with a dopant [are] selected from the group consisting of barium, strontium and titanium.

42. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

43. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

44. (Second Amended) The capacitor according to claim 43, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

45. (Second Amended) The capacitor according to claim 44, wherein the ratio of Ba to Sr is about 70:30.

46. (Second Amended) The capacitor according to claim 39, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

48. (Fifth Amended) A capacitor comprising:

a material layer having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation doped [a post deposition] doped BST high dielectric constant thin film material having a substantially uniform stoichiometry formed over [at least on both] said at least two sidewall regions and over said second level;

wherein [the stoichiometry of] said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level [substantially uniform at least at both sidewall regions]; and

a capping layer provided over at least a portion of said ion implantation doped BST thin film material.

50. (Second Amended) The capacitor according to claim 48, wherein [said dopants] said ion implantation doped BST thin film material is doped with a dopant [are] selected from the group consisting of barium, strontium and titanium.

51. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with a dopant selected from the group consisting of Ba and Sr.

52. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is doped with Ti.

53. (Second Amended) The capacitor according to claim 52, wherein said ion implantation doped BST high dielectric thin film material contains a Ti percentage of from about 50% to about 53.5% throughout said BST high dielectric thin film material.

54. (Second Amended) The capacitor according to claim 53, wherein the ratio of Ba to Sr is about 70:30.

55. (Second Amended) The capacitor according to claim 48, wherein said ion implantation doped BST high dielectric thin film material is included in a DRAM cell.

74. (Fifth Amended) An integrated circuit capacitor device comprising:

a first electrode [material layer] having a first level and a second level, said first and second levels being connected by at least two sidewall regions between said first and second levels; and

an ion implantation [a post deposition] doped BST high dielectric constant thin film material formed over [at least on both] said at least two sidewall regions and over said second level;

wherein [the stoichiometry of] said ion implantation doped BST high dielectric thin film material is a continuous layer at least on said two sidewall regions and said second level [substantially uniform at least at both sidewall regions]; and

a second electrode provided on said ion implantation doped BST high dielectric thin film [layer] material.